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Improving the Performance of Cascaded H-bridge based Interline Dynamic Voltage Restorer

Masoud Shahabadini, and Hossein Iman-Eini, *Member, IEEE*

***Abstract*—An interline dynamic voltage restorer (IDVR) is a new device for sag mitigation which is made of several dynamic voltage restorers (DVRs) with a common DC link, where each DVR is connected in series with a distribution feeder. During sag period, active power can be transferred from a feeder to another one and voltage sags with long durations can be mitigated. IDVR compensation capacity, however, depends greatly on the load power factor and a higher load power factor causes lower performance of IDVR. To overcome this limitation, a new idea is presented in this paper which allows to reduce the load power factor under sag condition, and therefore, the compensation capacity is increased. The proposed IDVR employs two cascaded H-bridge multilevel converters to inject AC voltage with lower THD and eliminates necessity to low-frequency isolation transformers in one side. The validity of the proposed configuration is verified by simulations in the PSCAD/EMTDC environment. Then, experimental results on a scaled-down IDVR are presented to confirm the theoretical and simulation results.**

***Index Terms*—Back-to-back converter, cascaded H-bridge, interline dynamic voltage restorer, minimum energy, power quality, voltage sag.**

NOMENCLATURE

V_{S_1}, V_{S_2}	source1 and source2 voltage
V_{L_1}, V_{L_1}	load1 and load2 voltage
V_{DVR_1}	DVR_1 injected voltage
V_{DVR_2}	DVR_2 injected voltage
V_{sag}	depth of voltage sag
V_{sag}^{max}	maximum depth of voltage sag
I_{L_1}, I_{L_2}	load1 and load2 current
S_{L_1}, S_{L_2}	load1 and load2 apparent power
P_{DVR}^{ME}	DVR active power based on minimum energy compensation method
φ	phase difference between the load voltage and the load current
α	phase difference between the load1 voltage and the source1 voltage during the sag period
β	phase difference between the load2 voltage and the source2 voltage during the sag period

I. INTRODUCTION

NOWADAYS, many efforts are done for power quality improvement. The voltage sag is one of the most significant power quality challenges for sensitive loads [1]. Depending on the magnitude and duration of the voltage sag, the resulting damages on industrial consumers are different [2], [3]. The high costs of these damages justify the increasing interest towards voltage sag mitigation techniques.

Dynamic voltage restorers (DVRs) are series type compensation devices which are used for voltage sag mitigation in the distribution system [4]. This device helps to maintain the load voltage close to the nominal value by injecting a series voltage to the supply network. Voltage sag compensation in the DVR can be achieved by purely reactive power injection or a combination of active and reactive power. But, a limited amount of voltage drop can be compensated by purely reactive power injection; hence, in most cases, it is necessary to transfer active power from a DC source such as a battery into AC line [5]. The compensation capacity in the DVR depends on the maximum achievable inverter voltage, the amount of stored energy in the DC link, voltage sag duration and its depth. Regarding these factors, several control strategies and circuit topologies have been presented in literature to improve the DVR performance [6]-[9].

Among the various compensation methods presented for control of a DVR, the in-phase compensation method and minimum energy strategy are more attractive [10], [11]. In the first one, the injected voltage is in-phase with the source voltage during the sag period. This method is simple and the injected voltage has the smallest magnitude. In the second method, the injected voltage is perpendicular to the load current, and therefore, the compensation method can work with minimum active power [12]. The ability of compensation with minimum energy is limited when the voltage sag exceeds a certain value, which is a function of the load power factor [6]. Although this approach reduces the energy consumption, the long term and deep voltage sags cannot be completely compensated just by reactive power injection. Hence, to have a comprehensive voltage sag compensation, it is necessary to employ active and reactive power injection into the distribution system. In other words, if the DC link of the DVR can be energized correctly, DVR will be able to mitigate deeper sags even with long durations.

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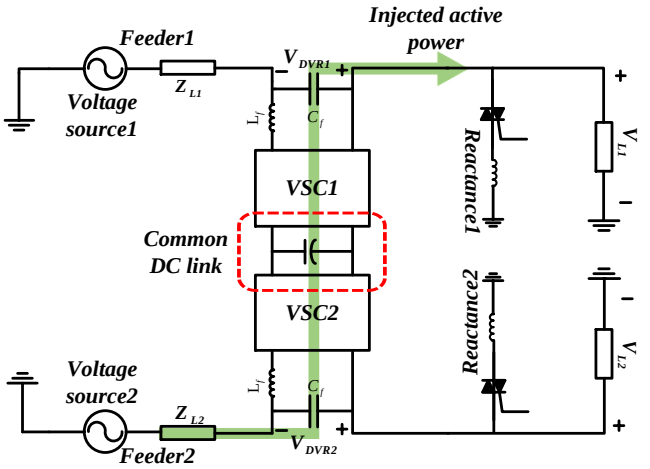

Fig. 1. Power circuit schematic of the IDVR with active power exchanging capability.

In [13], an interline DVR (IDVR) has been proposed. The structure of IDVR consists of several DVRs with a common DC link which protect sensitive loads against voltage sags, whereas each DVR has been located in an independent feeder. When one of the DVRs in IDVR structure starts to compensate the voltage sag by absorbing active power from the common DC link, the other ones operate in rectification mode and supply the DC link to maintain its voltage at a certain level.

In [14], a new control strategy for IDVR has been proposed which minimizes the rating of the power devices. Based on this strategy, a reduction in the cost and size of the IDVR without compromising its performance has been achieved.

In [15], an IDVR has been presented and instead of bypassing the DVRs in normal conditions, the DVRs are employed to improve the displacement factor (DF) of a specific feeder. This function is achieved by active and reactive power exchange (PQ sharing) between independent feeders.

In [16], a new configuration has been proposed which extends the capability of DVR to mitigate deeper voltage sags. This approach utilizes a shunt reactance parallel with the load to decrease the load power factor during the sag condition. In other words, much deeper voltage sags can be compensated when the load power factor is smaller.

As will be shown later, the performance of DVR (or IDVR) reduces at high power factors. For example, a DVR (or IDVR) with a capacitive DC link cannot compensate voltage sags which occur on the feeders with ohmic loads. To overcome this limitation, a topology is proposed in this paper which not only improves the capacity of IDVR in sag compensation at high power factors, but also improves the ability of compensator to mitigate very deep sags at moderate power factors. This goal is achieved by adding a reactance in parallel with each load to decrease the power factor intentionally during the sag condition.

In this paper, voltage sag compensation is done using an IDVR which employs two 7-level cascaded H-bridge (CHB) converters with a common DC link in the single phase mode.

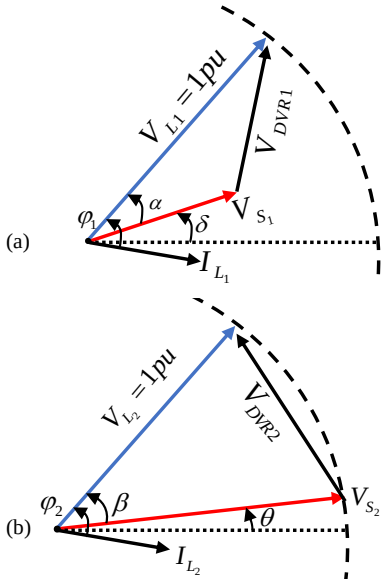

Fig. 2. Phasor diagram of IDVR during voltage sag compensation, (a) DVR1 injected voltage, (b) DVR2 injected voltage.

the authors employ the multilevel CHB converter for the first time in IDVR structure because of its modular topology and its interesting features for high-voltage and high-power applications. Finally, the validity of the proposed configuration and its effectiveness is verified by simulation and experimental results.

This paper is organized as follows; the operating principle of IDVR is given in section II, compensation scheme is presented in section III, the proposed IDVR structure is brought in section IV and the control strategy is shown in section V. Finally, the simulation and experimental results are given in section VI and section VII, respectively.

II. Operating Principle of IDVR

A simple IDVR which is shown in Fig. 1 consists of two back-to-back voltage source converters (VSC) with a common DC link. By using this topology, it is possible to transfer active power from a feeder to other one during the sag condition and to mitigate deeper and longer voltage sags (Fig. 1).

Consider, for example, the condition in which a voltage sag occurs in feeder1 and DVR1 starts to compensate it. Assuming P_{S1} and P_{L1} to be source1 and load1 active powers, then the injected active power by DVR1 would be

$$P_{DVR1} = P_{L1} - P_{S1} \tag{1}$$

using demonstrated phasor diagram in Fig. 2(a), (1) can be written as

$$P_{DVR1} = V_{L1} I_{L1} Cos(\varphi_1) - V_{S1} I_{L1} Cos(\varphi_1 - \alpha) \tag{2}$$

where it is obvious that load current I_{L1} is equal to source current I_{S1} due to series connection of DVR1 with load1.

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When minimum energy method is adopted for sag compensation, (2) is modified as,

$$P_{DVR1}^{ME}=\begin{cases}0 & if\ \ V_{S_1}\geq V_{L_1}Cos(\varphi_1)\\ V_{L_1}I_{L_1}(Cos(\varphi_1)-V_{S_1}/V_{L_1}) & if\ \ V_{S_1}<V_{L_1}Cos(\varphi_1)\end{cases} \quad (3)$$

Moreover, active power which is drown by DVR2 from feeder2 can be derived from Fig. 2(b) as follows,

$$P_{DVR2}=V_{L_2}I_{L_2}\left(Cos(\varphi_2-\beta)-Cos(\varphi_2)\right) \quad (4)$$

where injected voltage by DVR2 during sag period leads to a phase difference between $V_{L_2}$and V_{S_2} which is defined as β. According to (4) and [9], the maximum transferable active power is achieved when β is equal to φ_2 (phase of load2). In this condition, $Cos(\varphi_2-\beta)=1$ and (4) can be written as

$$P_{DVR2}^{\max}=V_{L_2}I_{L_2}(1-Cos(\varphi_2)) \quad (5).$$

Assuming that $S_{L_1}=\rho\, S_{L_2}$ and $V_{L_1}=I_{L_1}=1p.u$, β can be derived from (3) and (4) as

$$\beta=\begin{cases}0 & V_{sag}\leq 1-Cos(\varphi_1)\\ \varphi_2-Cos^{-1}(\rho Cos(\varphi_1)+Cos(\varphi_2)+\rho(V_{sag}-1)) & V_{sag}\geq 1-Cos(\varphi_1)\end{cases} \quad (6).$$

From (6), it is seen that for sag depth less than $1-Cos(\varphi_1)p.u.$, DVR2 is not involved to power exchange and just DVR1 compensates the sag. But, for sag values greater than $1-Cos(\varphi_1)p.u.$, DVR2 starts to exchange active power from feeder2 to feeder1 and participates in the compensation. In this case, the maximum value of β is φ_2 and the maximum voltage sag that can be compensated is obtained by

$$P_{DVR1}^{ME}\leq P_{DVR2}^{\max}\Rightarrow V_{sag}^{\max}=\frac{\rho+1}{\rho}-(Cos(\varphi_1)+\frac{1}{\rho}Cos(\varphi_2)) \quad (7).$$

In other words, for voltage sags greater than $V_{sag}^{max}p.u.$, IDVR is not capable to compensate it completely [13].

III. Proposed Compensation Scheme

According to (5), P_{DVR2}^{max} depends on the load power factor and at $Cos(\varphi_2)=1$, $P_{DVR2}^{max}=0$. In other words, the injection of active power is significantly limited at high power factors. From (7), it is also concluded that when $Cos(\varphi_1)$ and $Cos(\varphi_2)\approx 1$, then $V_{sag}^{max}\approx 0$. To overcome this problem and to improve the IDVR performance, the load power factor has to be decreased at the sag period. The remained question is that how to achieve this goal if the load power factor is higher than expected value. To resolve this issue, a thyristor-switched fixed value reactance is paralleled to each load. Using this reactance, one can decrease the load power factor when it is needed. In other words, when the IDVR capacity is not enough for compensation, the shunt reactances are added to the circuit. Otherwise, they are not employed in the compensation period.

To determine the value of shunt reactances, first the value of V_{sag}^{max} should be specified in the design step. Then, according to the loading of two feeders, the value of ρ is determined. Next, the value of load power factors $Cos(\varphi_1)$ and $Cos(\varphi_2)$ should be specified in (7). However, there is an equation with two unknowns and there is no forward rule for determining the power factors and consequently the value of shunt reactances. For solving this issue and getting sensible results on the design and analysis of IDVR, hereafter, it is assumed that the loading of two feeders are equal and $Cos(\varphi_1)=Cos(\varphi_2)=Cos(\varphi)$.

According to (7) and above assumptions, the effect of load power factor on the IDVR performance is obtained and demonstrated in Fig.3. It is observed that the ohmic loads (PF≈1) cannot be compensated completely by the IDVR because no β exists for these conditions. However, for loads with a lower power factor, IDVR can mitigate larger sags. For example, when the load power factor is 0.5, IDVR can compensate the whole range of voltage sags by choosing appropriate β. In other words, when feeder1 drops completely (or voltage sag amplitude is 1*p.u.*), IDVR can compensate it completely if the load power factor is 0.5.

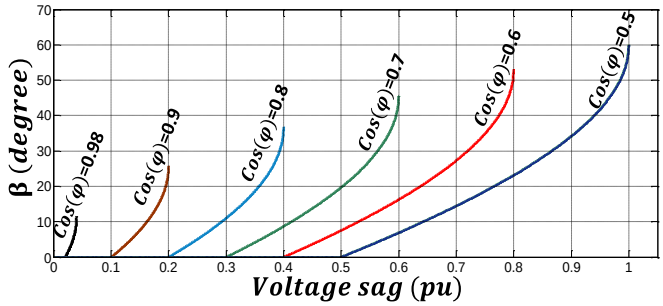

Fig. 3. Effect of load Power factor on the performance of IDVR.

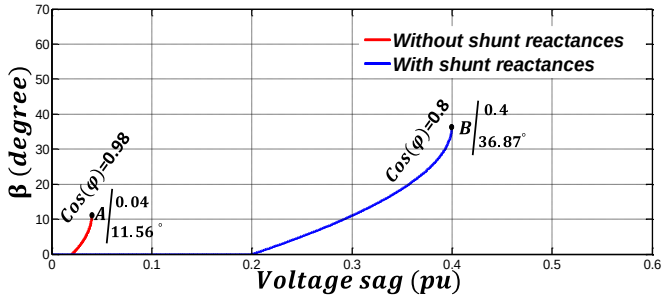

Fig. 4. IDVR performance improvement in the presence of shunt reactances.

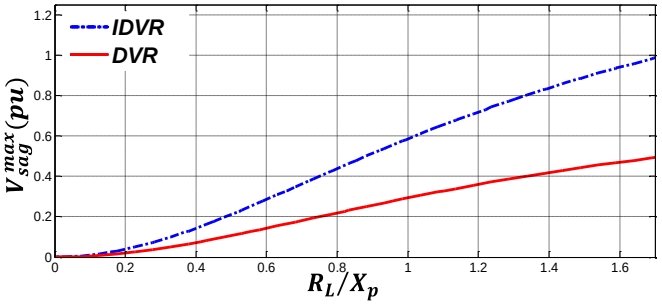

Fig. 5. Comparing the compensation capability of DVR and IDVR.

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Fig. 4 illustrates the improvement of IDVR compensation capability in the presence of shunt reactances. It is seen that by applying the shunt reactances and decreasing the power factor from 0.98 to 0.8, the depth of compensation increases from 0.04p.u. to 0.4p.u. (A & B points).

Fig. 5 shows a comparison between the compensation capability of two separate DVRs and an IDVR for different R_L/X_p ratios. The first topology consists of two independent DVRs installed on feeder1 and feeder2 with capacitive DC links [16]. To extract the corresponding curve of compensation capacity, it is assumed that the load power factor is 1, $R_L = 1p.u.$ and the shunt impedance is X_p. Then using (3), one can write:

$$V_{sag} \le 1 - Cos(\varphi) \tag{8}$$

$$Cos(\varphi) = \frac{1}{\sqrt{1+(R_L/X_p)^2}} \tag{9}$$

and

$$V_{sag}^{\max} = 1 - \frac{1}{\sqrt{1+(R_L/X_p)^2}} \tag{10}$$

which is depicted in Fig. 5 with solid line for various R_L/X_p ratios.

Second topology is an IDVR that is built from the same DVRs with a common DC link. With a similar methodology, one can obtain:

$$P_{DVR1}^{ME} \le P_{DVR2}^{\max} \quad \Rightarrow \quad V_{sag} \le 2 - 2Cos(\varphi) \tag{11}$$

Therefore

$$V_{sag}^{\max} = 2 - \frac{2}{\sqrt{1+(R_L/X_p)^2}} \tag{12}$$

which is depicted in Fig. 5 with dot-and-dash line for different R_L/X_p ratios.

Comparing (10) with (12) reveals that the compensation capability of IDVR is twice the two separate DVRs for different R_L/X_p ratios.

It is worth mentioning that adding a reactance in parallel to the load increases IDVR rating, but it helps to compensate deep voltage sags. In other words, the cost of compensating deep voltage sag is the increase of IDVR rating. Hence, a tradeoff has to be done among the additional cost, the IDVR rating, and the maximum compensable voltage sag.

The worst condition for voltage and current rating of IDVR occurs when the loads are ohmic. Consider, for example, the maximum IDVR current rating should not exceed γ p.u. from the load nominal current, i.e., 1p.u. Then one can write:

$$1+\gamma = \left| \frac{1}{R_L \,||\, jX_p} \right|^{R_L = 1pu} = \sqrt{1+(R_L/X_p)^2} \tag{13}$$

and by inserting (13) into (12), the maximum compensable voltage sag can be derived as

$$V_{sag}^{\max} = \frac{2\gamma}{1+\gamma} \tag{14}$$

Based on the phasor diagram depicted in Fig. 2(a), the DVR injected voltage is obtained by using the following equation

$$V_{DVR_1} = \sqrt{V_{S_1}^2 + V_{L_1}^2 - 2V_{S_1}V_{L_1}Cos(\alpha)} \tag{15}$$

where its maximum value affects on the IDVR voltage rating. In the minimum energy compensation method, the value of V_{DVR_1} is maximum when $\alpha = \varphi$. After adding shunt reactance and with respect to (13), φ is derived as

$$\varphi = 90 - tan^{-1}\left(\frac{1}{\sqrt{\gamma^2+2\gamma}}\right) \tag{16}$$

Now using (14) and (16), (15) is rewritten as

$$V_{DVR_1} = \sqrt{\frac{2(1+\gamma^2)}{(1+\gamma)^2} - 2\left(\frac{1-\gamma}{1+\gamma}\right)Sin\left(tan^{-1}\left(\frac{1}{\sqrt{\gamma^2+2\gamma}}\right)\right)} \tag{17}$$

where (17) can be used to determine the voltage rating of voltage source converters in the IDVR. Consequently, from the design point of view, first, γ should be determined from (14), then X_P value and the IDVR current and voltage rating are obtained with respect to this parameter. According to the above equations, it is obvious that greater V_{sag}^{max} leads to greater γ and therefore greater IDVR rating.

IV. CHB Based IDVR

Most of the published literature in the field of DVR and IDVR deal with voltage source converters realized using two-level converters. But, in high-voltage and high-power applications, a CHB based multilevel converter is a more attractive solution and its application in an IDVR is introduced in this paper. Among the multilevel topologies, cascaded H-bridge converter is more interested for IDVR topology because of its modular structure, reaching medium output voltage levels using only standard low voltage mature technology components, and the higher reliability. Moreover, low frequency modulation techniques and fault-tolerant algorithms can be easily applied in the CHB based IDVRs [17]-[19].

In a CHB converter, depending on the number of voltage levels which has to be synthesized, separate DC links are needed. In IDVR structure, however, by back-to-back

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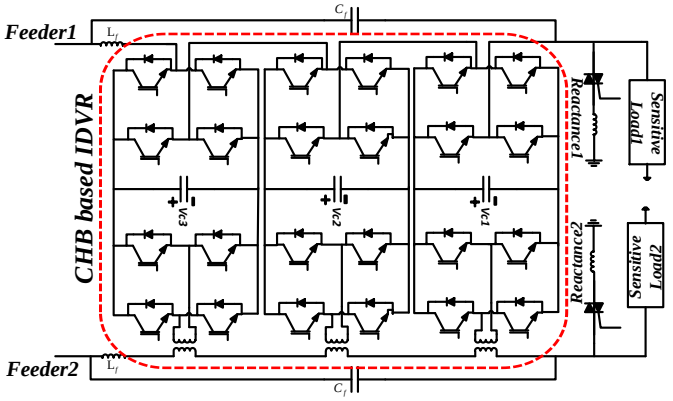

Fig. 6. Proposed IDVR structure.

connection of two CHB converters and use of low frequency isolation transformers in one side, distinct DC links are easily provided. Furthermore, this structure eliminates the necessity to isolation transformers in one side which leads to lower size, weight and cost. The number of H-bridge cells in a CHB converter is chosen according to the required AC voltage and the voltage rating of power switches. Fig. 5 demonstrates a single phase 7-level CHB based IDVR which is used in simulation study and experimental investigation. Although a 7-level back-to-back converter is chosen for the study in this paper, the proposed control strategy can be applied to any number of voltage levels and there is no limitation from this point of view. In other words, the generated voltage references by the control system will be synthesized by the CHB converter through well-known multilevel modulation techniques. The only issue is related to keeping voltage balance among DC link capacitors which has been addressed in [17] and [20] for any number of voltage levels.

In the utilized 7-level CHB converter, the DC link voltage and current rating of each cell can be specified with respect to (13) and (17). Assuming DC link utilization factor is 0.85, then each cell current and its DC link voltage must be greater than $1+\gamma$ and $V_{DVR_1}/(3\times 0.85)$ respectively.

V. Implementation of Control Strategy

As was already mentioned, the minimum energy strategy is utilized for voltage sag compensation in this paper. Based on this method, the block diagram of the control system is shown in Fig. 7. In this control strategy, first the magnitude of voltage sag is calculated and compared with $2-2Cos(\varphi)_{old}$. If the sag amplitude is greater than this value, then the shunt reactances are paralleled to the loads to decrease the load power factor. Next, with respect to equivalent power factor which is seen by the source, the DVR voltages are determined. This control system needs a fast and accurate estimation system for calculation of phase and magnitude of corresponding waveforms. Among the estimation methods which have been proposed in literature ([21], [22]), the fast fourier transform (FFT) is the most common one and presents relatively good accuracy [23]. In this paper, FFT algorithm is therefore used for estimation of $v_{s_1}(t), v_{s_2}(t), i_{L_1}(t)$ and $i_{L_2}(t)$. After estimation of these signals, the control system is

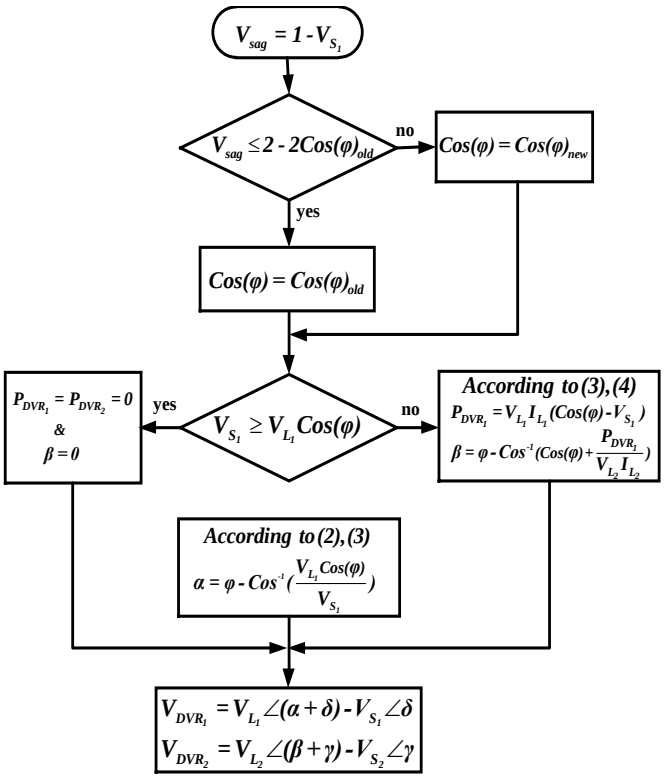

Fig. 7. Flowchart of the IDVR control system.

TABLE I
PARAMETERS OF THE UTILIZED IDVR FOR SIMULATION

Parameters	Value
Modulation	Phase Shifted PWM
Switching frequency	1KHz
PFs of the loads (High PF condition)	0.98
PFs of the loads (Fairly moderate PFs)	0.8
Total DC-link voltage	7.5Kv
Rated voltage	6.351Kv
DC-link capacitor (per H-bridge)	2000uF
Shunt inductances (High PF condition)	0.23H
Shunt inductances (Fairly moderate PFs)	1.02H

able to detect voltage sags and mitigate them by producing the appropriate reference signals for the IDVR (Fig. 7).

VI. Simulation Results

To investigate the system performance in voltage sag compensation, several simulations have been done in the PSCAD/EMTDC environment on a single-phase IDVR similar to that in Fig. 6. In these simulations, two shunt reactances are used for power factor reduction during the sag periods. By adding the shunt reactances, DC-current component may occur, however, if the shunt reactance is switched on at near the peak of the voltage, this component will be significantly small. The parameters of the understudy system are listed in Table I.

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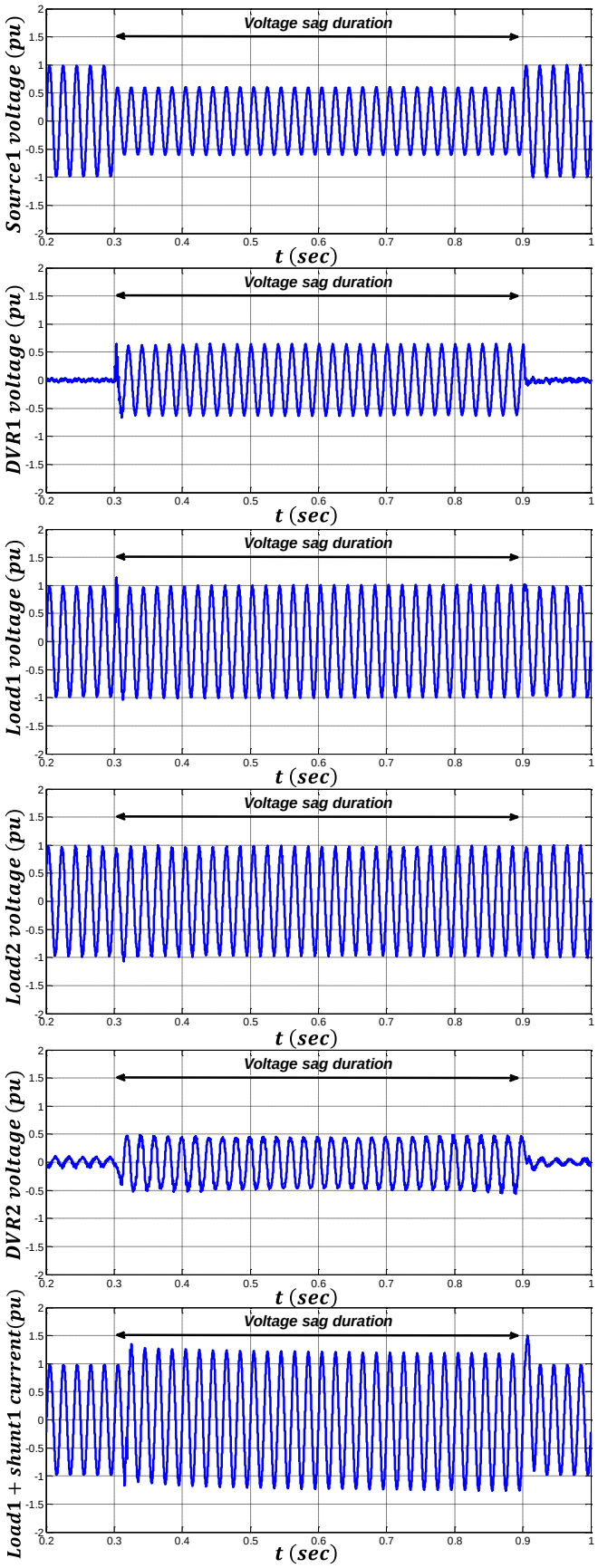

Fig. 8. Investigating the IDVR performance when the proposed method is applied for a sag with depth of 0.4p.u.

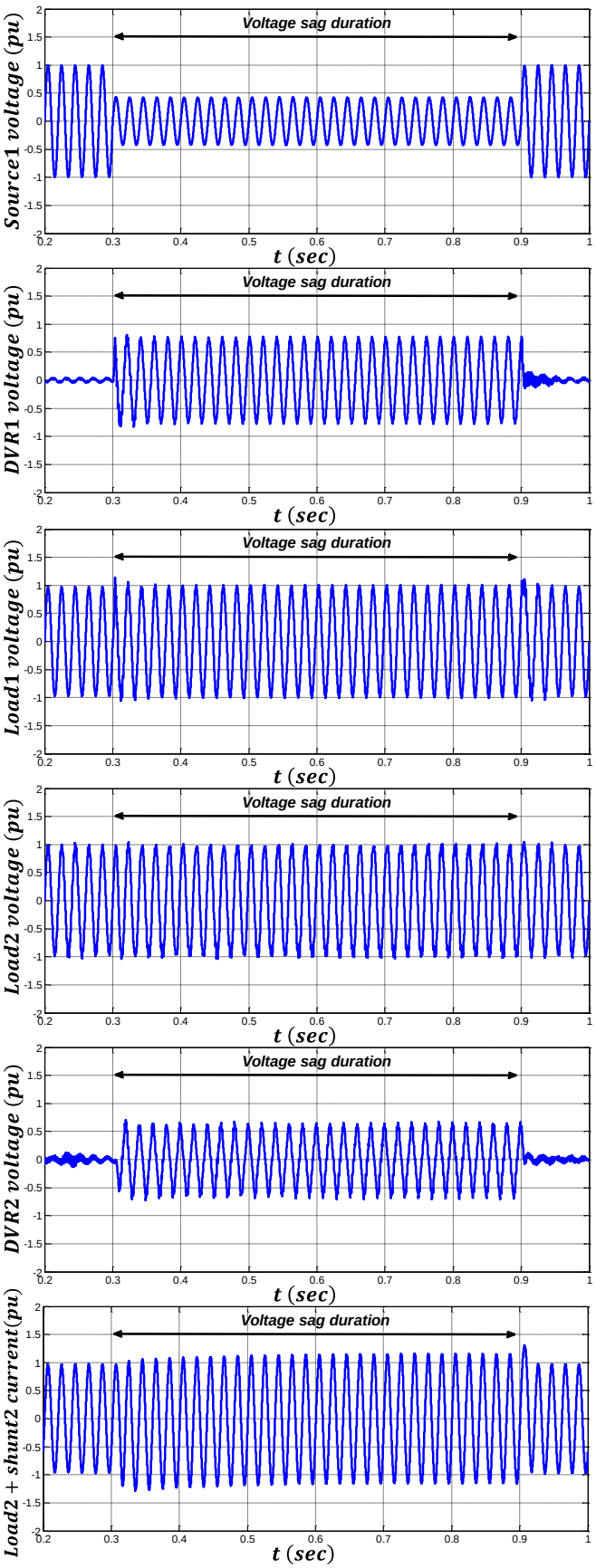

Fig. 9. Investigating the IDVR performance when the proposed method is applied for a sag with depth of 0.6p.u.

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A. *Compensation at High Power Factors*

In this study, a sag with the depth of 0.4p.u. occurs on the source1 at t=0.3s. As was already mentioned, at high power factors, the ordinary IDVR is not able to mitigate such kind of voltage sags. However, after inserting the shunt ractances and reducing the load power factors from 0.98 to 0.8, the IDVR can compensate this voltage sag completely as it can be seen in Fig. 8.

B. *Fairly Moderate Power Factors*

In this part, the power factors of both loads are reduced from 0.8 to 0.7 during the sag condition. According to (11), at this condition the IDVR can compensate the voltage sags with the maximum depth of 0.6p.u. Fig. 9 illustrates the IDVR operating principle when the proposed configuration is employed. It can be seen that the IDVR can successfully compensate the voltage sag and keep the load voltage at 1p.u. Table II provides a numerical example to compare the proposed IDVR performance with two separate DVRs installed at the same feeders. In this comparison, similar to previous study, the load power factors are reduced from 0.8 to 0.7 during sag period. The obtained results in Table II show that the proposed IDVR topology can compensate larger amount of voltage sags.

TABLE II
COMPARING THE COMPENSATION CAPABILITY OF VARIOUS TOPOLOGIES

	Ordinary DVR	DVR with shunt reactance	Ordinary IDVR	IDVR with shunt reactances
$V_{sag}^{max}\ (pu)$	0.2	0.3	0.4	0.6

VII. EXPERIMENTAL RESULTS

The laboratory prototype of the implemented IDVR is shown in Fig. 10. It has the structure similar to Fig. 6 and its parameters are listed in Table III. The processor of the control system is a STM32F407VG ARM microcontroller.

Similar to the case study in the simulation part, a 40% voltage sag is applied to the voltage source1. Fig. 11 shows corresponding waveforms, before and after the voltage sag. It is seen that the IDVR can compensate the voltage sag completely with the help of shunt reactances. These experimental results have been carried out only for the high power factor condition which was mentioned in simulation study.

By observing DVR1 injected voltage, it is seen that V_{DVR1} is not entirely zero before the voltage sag. This small voltage is produced to prepare the initial charge of DC link capacitors and maintain them in the desired value.

Moreover, it is seen that before the voltage sag occurrence, the shunt reactances are not in the circuit and $i_{reactance1} = i_{reactance2} = 0$. But, after sag condition, they are switched into the circuit and help to reduce the load power factor from 0.98 to 0.8.

TABLE III
PARAMETERS OF THE UNDER EXPERIMENT SYSTEM

Parameters	Value
Modulation	Phase Shifted PWM
Switching frequency	1kHz
PFs of the loads	0.98
Total DC-link voltage	66v
Rated voltage (rms)	60v
DC-link capacitor (per H-bridge)	400uF
Shunt inductances	225mH
Load resistance	52ohm

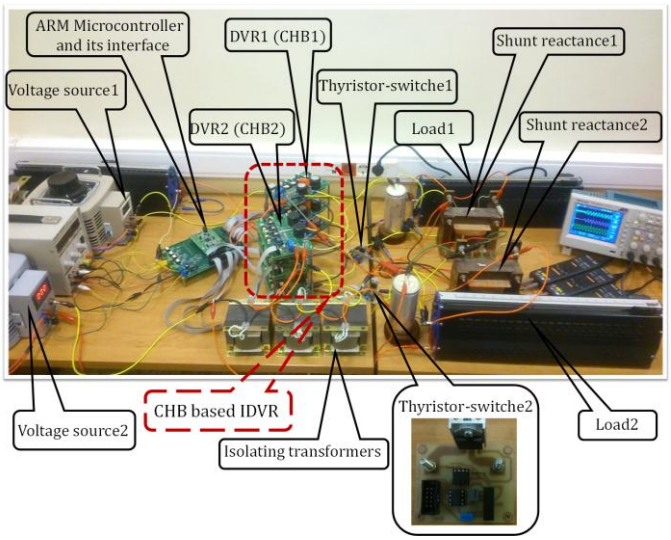

Fig. 10. Laboratory hardware prototype of the IDVR system.

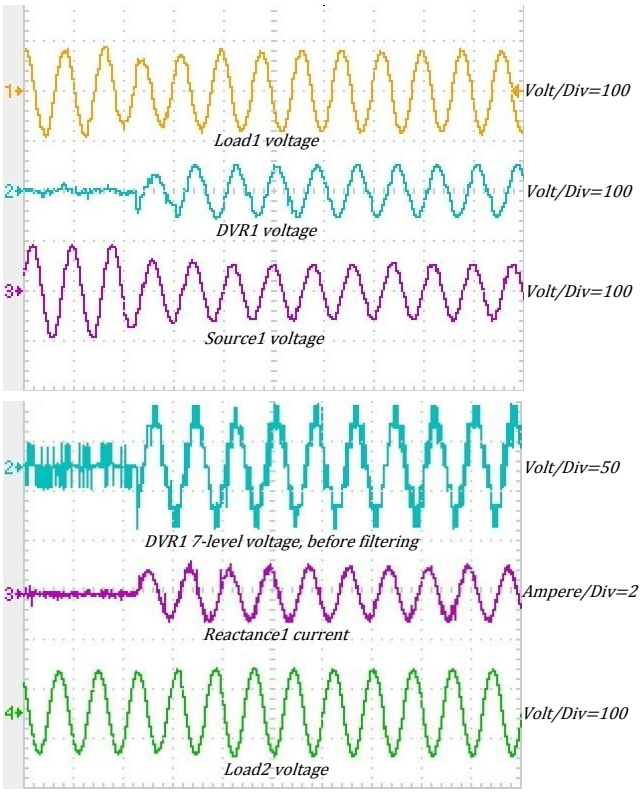

Fig. 11. Experimental results for the voltage restoration function.

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VIII. Conclusion

In this paper, a new configuration has been proposed which not only improves the compensation capacity of the IDVR at high power factors, but also increases the performance of the compensator to mitigate deep sags at fairly moderate power factors. These advantages were achieved by decreasing the load power factor during sag condition. In this technique, the source voltages are sensed continuously and when the voltage sag is detected, the shunt reactances are switched into the circuit and decrease the load power factors to improve IDVR performance. Finally, the simulation and practical results on the CHB based IDVR confirmed the effectiveness of the proposed configuration and control scheme.

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Masoud Shahabadini was born in Kerman, Iran, in 1990. He received the B.Sc. degree in Electrical Engineering from the Shahid Bahonar University of Kerman, Kerman, Iran, in 2012, and the M.Sc. degree in Electrical Engineering from the University of Tehran, Tehran, Iran, in 2015 where he is pursuing the Ph.D. degree in electrical engineering. His research interests include multilevel converters, power quality, and power electronics application in power systems.

Hossein Iman-Eini received his B.S. and M.S. from the University of Tehran, Tehran, Iran, in 2001 and 2003, respectively, and his Ph.D. from both the University of Tehran and the Grenoble Institute of Technology, France, in 2009, all in Electrical Engineering. He is currently an Assistant Professor in the School of Electrical and Computer Engineering, University of Tehran. His current research interests include the modeling and control of power converters, multilevel converters and renewable energy systems.